Claims

1. A method, comprising:

setting a status corresponding to a block of data in response to a change in address mapping to indicate that the block of data is pending write back.

2. The method of claim 1, further including changing the address mapping in response to switching from executing a first software process to executing a second software process, wherein the first software process uses a first address mapping and the second software process uses a second address mapping.

3. The method of claim 2, further comprising preventing access to the block of data by the second software process while the status is set.

4. The method of claim 2, wherein setting includes setting the status to indicate that the block of data is not accessible to the second software process.

5. The method of claim 2, wherein setting includes setting the status to indicate that the block of data is not accessible using the second address mapping.

6. The method of claim 2, wherein the status is a bit in a cache tag field and wherein the cache tag field includes information associated with the block of data, and wherein setting includes setting the bit in response to the change in address mapping to indicate that the block of data is pending write back from a first level of a memory hierarchy to a second level of the memory hierarchy and to indicate that the block of data in the first level of the memory hierarchy is not accessible with the current address mapping.

7. The method of claim 1, wherein the status is a bit in a cache tag field, wherein the cache tag field includes information associated with the block of data that is stored in a cache memory, and wherein setting the bit includes setting the bit if the block of data is valid and dirty.

8. The method of claim 7, wherein setting includes setting the bit in the cache tag field if a valid bit of the cache tag field is set and if a dirty bit of the cache tag field is set, wherein the dirty bit indicates if the block of data has been modified while in the cache memory and the valid bit indicates if the block of data is valid.

9. The method of claim 1, further comprising writing back the block of data from a first level of memory to a second level of the memory using either a demand driven write back scheme or a lazy write back scheme.

10. An apparatus, comprising:

a storage area to store a status associated with a block of data to indicate that the block of data is pending write back and is not accessible with the current address mapping.

11. The apparatus of claim 10, wherein the status is encoded in at least one bit in a cache tag.

12. The apparatus of claim 11, wherein the block of data is cache data stored in a first level of a memory hierarchy and the at least one bit indicates that the block of data is pending write back to a second level of the memory hierarchy.

13. The apparatus of claim 12, wherein the first level of the memory hierarchy is an inner cache and the second level of the memory hierarchy is an outer cache.

14. The apparatus of claim 12, wherein the cache tag includes a valid bit to indicate if the block of data is valid and a dirty bit to indicate if the block of data has been modified while in the first level of the memory hierarchy.

15. The apparatus of claim 14, wherein the apparatus further includes digital logic to set the at least one bit if the valid bit is set and the dirty bit is set.

16. The apparatus of claim 11, wherein the apparatus further includes digital logic to set the at least one bit in response to a change in address mapping.

17. The apparatus of claim 10, wherein the storage area is located in a cache memory.

18. The apparatus of claim 17, wherein the cache memory is an static random access memory (SRAM).

19. The apparatus of claim 10, wherein the apparatus is a processor.

20. The apparatus of claim 19, wherein the processor includes logic to translate virtual addresses to physical addresses.

21. The apparatus of claim 10, wherein the apparatus is a virtually addressed cache memory.

22. The apparatus of claim 10, wherein the apparatus is a virtually addressed buffer.

23. An apparatus, comprising:

a storage area to store information about a predetermined amount of data, wherein the information indicates if the predetermined amount of data is awaiting a write back and the information is updated in response to a change in address mapping.

24. The apparatus of claim 23, wherein the information is at least one bit in a cache tag.

25. The apparatus of claim 24, wherein the predetermined amount of data is cache data stored in a first level of a memory hierarchy and the at least one bit indicates that the block of data is awaiting write back to a second level of the memory hierarchy.

26. The apparatus of claim 25, wherein the cache tag includes a valid bit to indicate if the predetermined amount of data is valid and a dirty bit to indicate if the predetermined amount of data has been modified while in the first level of the memory hierarchy and wherein the apparatus further includes digital logic to set the at least one bit if the valid bit is set and the dirty bit is set.

27. The apparatus of claim 26, wherein the address mapping is changed in response to switching from executing a first software process to executing a second software process and wherein the apparatus further includes digital logic to prevent access to the predetermined amount of data by the second software processes while the at least one bit is set.

28. The apparatus of claim 23, wherein the address mapping is changed in response to switching from executing a first software process to executing a second software process and wherein the apparatus further includes digital logic to prevent access to the predetermined amount of data by the second software process while the predetermined amount of data is awaiting the write back.

29. The apparatus of claim 23, wherein the apparatus is a processor and the processor includes logic to translate virtual addresses to physical addresses.

30. The apparatus of claim 23, wherein the apparatus is a virtually addressed cache memory.

31. The apparatus of claim 23, wherein the apparatus is a virtually addressed buffer.

32. A method, comprising:

setting at least one bit to prevent access to a predetermined amount of data stored in a first level of a memory while the predetermined amount of data is pending a write back to a second level of the memory.

33. The method of claim 32, wherein setting includes setting the at least one bit to in response to a change in address mapping, wherein the at least one bit indicates that the predetermined amount of data is pending a write back to the second level of memory, wherein the first level of memory is a virtually addressed cache memory and the predetermined amount of data is a line of cache data.

34. The method of claim 32, wherein the first level of the memory is a cache memory and further including storing the at least one bit in the cache memory.

35. A method, comprising:

setting a dirty bit in a cache tag that is associated with a predetermined amount of cache data; and

setting a write back bit in the cache tag.

36. The method of claim 35, further comprising setting a valid bit in the cache tag and wherein the write back bit is set if the dirty bit is set and if the valid bit is set.

37. The method of claim 36, further comprising setting the write back bit in response to a change in address mapping in a virtually addressed system.

38. The method of claim 35, wherein the predetermined amount of data is a line of cache data stored in a first level of a memory hierarchy and wherein the write back bit indicates that the cache data is pending a write back to a second level of the memory hierarchy and wherein the dirty bit indicates that the block of data has been modified while in the first level of the memory hierarchy.

39. An apparatus, comprising:

a circuit to set at least one bit in response to a change in address mapping and to indicate if a predetermined amount of data is pending a write back.

40. The apparatus of claim 39, wherein the predetermined amount of data is stored in a first level of a memory hierarchy and wherein the circuit is adapted to prevent access to the predetermined amount of data stored in the first level of the memory hierarchy while the predetermined amount of data is pending a write back to a second level of the memory hierarchy.

41. The apparatus of claim 40, wherein the apparatus is the processor.

42. The apparatus of claim 41, wherein the processor includes logic to translate virtual addresses to physical addresses, the first level of the memory hierarchy is a cache memory, the predetermined amount of data is a line of cache data, and the at least one bit is in a cache tag field associated with the line of cache data and the at least one bit is stored in the cache memory.

43. A system, comprising:

a circuit to set at least one bit in response to a change in address mapping and to indicate if a predetermined amount of data is pending a write back; and

an antenna coupled to the first processor.

44. The apparatus of claim 43, wherein the circuit is adapted to prevent access to the predetermined amount of data stored in a first level of a memory hierarchy while the predetermined amount of data is pending a write back to second level of the memory hierarchy.

45. The apparatus of claim 44, wherein the system includes a processor that includes the circuit, the processor includes logic to translate virtual addresses to physical addresses, the first level of the memory hierarchy is a cache memory, the predetermined amount of data is a line of cache data, and the at least one bit is in a cache tag field associated with the line of cache data and the at least one bit is stored in the cache memory.

46. The system of claim 43, wherein the system is a wireless phone.